REMARKS

Please cancel Claim 3 without prejudice. Claims 1, 7-8, 10, 12-13 and 21-25 are pending. Claims 1, 10 and 21 are amended herein. No new matter is added as a result of the claim amendments. Support for the claim amendments can be found at least in Figures 2A, 2B and 2C of the instant application.

Claim Objection

Claims 1 and 21 are objected to for the reasons cited in the instant Office Action. Claims 1 and 21 are amended to address the objection.

102 Rejections

The instant Office Action states that Claims 1, 10, 12 and 21-23 are rejected under 35 U.S.C. § 102(e) as being anticipated by Bhattacharyya (U.S. Patent No. 6,713,810; hereinafter "Bhattacharyya '810"). The Applicants have reviewed the cited reference and respectfully submit that the present invention as recited in Claims 1, 10, 12 and 21-23 is not anticipated nor rendered obvious by Bhattacharyya '810.

Applicants respectfully submit that Bhattacharyya '810 does not show or suggest the particular memory cell structures recited in independent Claims 1, 10 and 21. That is, Applicants respectfully submit that Bhattacharyya '810 does not show or suggest "a dielectric layer sandwiched between and adjoining both said silicon dioxide layer and said floating gate, said dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide" as recited in independent Claim 1, nor does Bhattacharyya '810 does not show or suggest "a tunnel oxide layer sandwiched between and adjoining both said substrate

AMD-H0561/JPH/WAZ Examiner: NGUYEN, D. Serial No.: 10/658,936 Group Art Unit: 2818 and said first layer, said tunnel oxide layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide" as recited in independent Claim 10, nor does Bhattacharyya '810 does not show or suggest "a dielectric layer sandwiched between and adjoining both said first layer and said second layer, said dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide" as recited in independent Claim 21.

Therefore, Applicants respectfully submit that independent Claims 1, 10 and 21 are in condition for allowance. As such, Applicants also respectfully submit that Bhattacharyya '810 does not show or suggest the additional claimed features of the present invention as recited in Claims 12 and 22-23 dependent on either Claim 10 or 21, and that Claims 12 and 22-23 are also in condition for allowance as being dependent on allowable base claims. As such, the Applicants respectfully assert that the basis for rejecting Claims 1, 10, 12 and 21-23 under 35 U.S.C. § 102(e) is traversed.

103 Rejections

The instant Office Action states that Claims 7-8, 13 and 24-25 are rejected under 35 U.S.C. § 103(a) as being anticipated by Bhattacharyya '810 in view of Bhattacharyya (U.S. Patent No. 6,784,480; hereinafter "Bhattacharyya '480"). The Applicants have reviewed the cited references and respectfully submit that the present invention as recited in Claims 7-8, 13 and 24-25 is not anticipated nor rendered obvious by Bhattacharyya '810 and Bhattacharyya '480, alone or in combination.

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As presented above, Applicants respectfully submit that Bhattacharyya '810 does not show or suggest the present invention as recited in independent Claims 1, 10 and 21. Claims 7-8, 13 and 24-25 are dependent on either Claim 1, 10 or 21 and recite additional limitations. Hence, by demonstrating that Bhattacharyya '810 and Bhattacharyya '480, alone or in combination, do not show or suggest the limitations of Claims 1, 10 and 21, it is also demonstrated that Bhattacharyya '810 and Bhattacharyya '480, alone or in combination, do not show or suggest the limitations of Claims 7-8, 13 and 24-25.

Applicants respectfully submit that Bhattacharyya '480 does not show or suggest the particular memory cell structures recited in independent Claims 1, 10 and 21. That is, Applicants respectfully submit that Bhattacharyya '480, alone or in combination with Bhattacharyya '810, does not show or suggest "a dielectric layer sandwiched between and adjoining both said silicon dioxide layer and said floating gate, said dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide" as recited in independent Claim 1, "a tunnel oxide layer sandwiched between and adjoining both said substrate and said first layer, said tunnel oxide layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide" as recited in independent Claim 10, nor "a dielectric layer sandwiched between and adjoining both said first layer and said second layer, said dielectric layer comprising a dielectric material having a dielectric constant greater than that of silicon dioxide" as recited in independent Claim 21.

Therefore, Applicants also respectfully submit that Bhattacharyya '810 and Bhattacharyya '480, alone or in combination, do not show or suggest the additional

AMD-H0561/JPH/WAZ Serial No.: 10/658,936 Examiner: NGUYEN, D. 7 Group Art Unit: 2818 claimed features of the present invention as recited in Claims 7-8, 13 and 24-25 dependent on either Claim 1, 10 or 21, and that Claims 7-8, 13 and 24-25 are also in condition for allowance as being dependent on allowable base claims. As such, the Applicants respectfully assert that the basis for rejecting Claims 7-8, 13 and 24-25 under 35 U.S.C. § 103(a) is traversed.

Conclusions

In light of the above remarks, Applicants respectfully request reconsideration of the rejected claims.

Based on the arguments presented above, Applicants respectfully assert that Claims 1, 7-8, 10 and 12-13 and 21-25 overcome the rejections of record and, therefore, Applicants respectfully solicit allowance of these claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Date: [0 (8)05

Respectfully submitted,

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